

IN THE SPECIFICATION:

Please amend paragraph [0001] as follows:

[0001] Field of the Invention: The present invention relates to semiconductor devices and, more particularly, to threshold voltage adjustment of ~~long channel~~ long-channel MOS transistors.

Please amend paragraph [0005] as follows:

[0005] The threshold voltage of transistor 10 may be altered or adjusted by implanting the surface of substrate 16 in channel region 18 with, for example, a p-type dopant which, in turn, decreases the number of electrons that can be accumulated at the surface in the channel region 18. Since fewer electrons are available, a higher gate voltage is needed to attract the minimum number of electrons that are required to form an inversion layer in the channel region 18. A threshold voltage adjustment implant is commonly referred to as an “enhancement” implant.

Please amend paragraph [0006] as follows:

[0006] MOS transistors are formed using photolithographic processes according to design rules corresponding to a particular process. The design rules specify, among other things, the minimum length of the channel region. To gain performance advantages and as processing technology advancements have been achieved, the channel length between the source and drain has generally shortened. Furthermore, to minimize the silicon area consumed by an MOS circuit, a typical integrated circuit design is largely implemented with transistors that have the minimum channel length. Since the circuit is largely implemented with transistors that have the minimum channel length, the fabrication process, for example the enhancement implant, is commonly optimized to adjust the threshold voltages of the transistors which have the minimum channel length. While performance improvement is generally a paramount objective for MOS circuit design, it is common for circuits, in addition to utilizing transistors having minimum channel length, to also require transistors which have channel lengths that are longer than the minimum.

For those transistors with a longer channel length, a lower threshold voltage is realized when the threshold voltage is optimized for a ~~shorter channel~~ shorter channel transistor through the use of a single enhancement implant.

Please amend paragraph [0008] as follows:

[0008] One prior solution to this problem is to utilize multiple threshold voltage adjusting enhancement implants. In a first step, dopants are implanted into the surface of the substrate to adjust the threshold voltages of the ~~short channel~~ short channel transistors while the ~~long channel~~ long channel transistors are protected from the implant. In a second step, dopants are implanted into the surface of the substrate to adjust the threshold voltages of the long or longer channel transistors while the short-channel transistors are protected from the implant. By utilizing, for example, two implant steps, the dopant concentration for the short and long channel lengths can be separately optimized.

Please amend paragraph [0010] as follows:

[0010] The present invention, in exemplary embodiments, is directed to threshold voltage adjustments for ~~long channel~~ long channel transistors fabricated using processes optimized for ~~short channel~~ short channel transistors. In one embodiment of the present invention, a threshold-adjusted transistor includes a substrate with spaced-apart source and drain regions formed in the substrate and a channel region defined between the source and drain regions. A layer of gate oxide is formed over at least a part of the channel region with a gate formed over the gate oxide. The gate further includes at least one implant aperture formed therein with the channel region of the substrate further including an implanted region within the channel between the source and drain regions.

Please amend paragraph [0012] as follows:

[0012] In yet another embodiment of the present invention, a method is provided for adjusting a threshold voltage of a ~~long channel~~ long channel transistor in a fabrication process

optimized for short-channel transistors. At least one aperture is formed in a gate on a substrate with a first dopant implanted through the at least one aperture into a channel region of the substrate. The first implanted dopant is annealed into the channel of the ~~long-channel~~ long-channel transistor.

Please amend paragraph [0013] as follows:

[0013] In yet a further embodiment of the present invention, a method for manufacturing a MOS- an MOS structure on a semiconductor substrate is provided. A gate oxide layer is formed over the semiconductor substrate with a polysilicon layer also being formed over the gate oxide layer. A first mask layer is formed and patterned followed by etching to form a gate. The gate includes an aperture between the source and drain ends of the polysilicon layer. Implant regions are formed in the substrate adjacent to the drain and source ends of the gate. Also, at least one implant region is formed in the substrate through the aperture of the gate. Source and drain regions are formed in the substrate adjacent to the source and drain ends of the gate.

Please amend paragraph [0023] as follows:

[0023] While ~~short-channel~~ short-channel transistors are susceptible to decreased threshold voltages and therefore utilize threshold voltage adjusting enhancement implants for adjusting the threshold voltage, ~~short-channel~~ short-channel transistors are also susceptible to so-called "hot carrier effects." Generally, as the channel length is shortened, the maximum electric field E_m becomes more isolated near the drain side of the channel, causing a saturated condition that increases the maximum energy on the drain side of the MOS device. The high energy causes electrons in the channel region to become "hot." An electron generally becomes hot in the vicinity of the drain edge of the channel where the energy arises. Hot electrons can degrade device performance and cause breakdown of the device. Moreover, the hot electrons can overcome the potential energy barrier between the silicon substrate and the silicon dioxide layer overlying the substrate, which causes hot electrons to be injected into the gate oxide.

Please amend paragraph [0027] as follows:

[0027] In addition to the concern over hot carrier injection in short channels, a condition known as “punch-through” is also of concern. To further protect the transistor from punch-through conditions, a double diffusion (DD) process may further surround the LDDs. The DD process implants one or more dopants into the same region followed by a high temperature annealing step, in which the one or more dopants diffuse simultaneously, and form a structure called a ~~double-diffused~~ double-diffused (DD) region, also commonly called a double-diffused drain (DDD). In an exemplary DD process, a medium phosphorus dose and a heavy arsenic dose may be implanted; but in both cases a p-type Boron halo implant is put in to surround the n-type LDD implant to protect against ~~“punch-through.”~~ “punch-through.” The faster-diffusing phosphorus is driven farther under the gate edge than the arsenic, creating a less abrupt concentration gradient for the drain.

Please amend paragraph [0029] as follows:

[0029] FIG. 3 is a perspective view of a transistor incorporating a channel implant process, in accordance with an embodiment of the present invention. A transistor 30 is formed upon and within a substrate 42 and generally includes a gate 32 formed upon a gate oxide 28 according to processes known by those of ordinary skill in the art. Transistor 30 further includes a drain region 48 and a respective source region 50 generally formed within substrate 42. In accordance with the channel implant process of an embodiment of the present invention, gate 32 further includes one or more apertures 34, 36 formed within the general body of gate 32. Apertures 34, 36 provide internal implant windows 38, 40 into the channel region 52 located generally below gate 32. The quantity of apertures 34, 36 is a function of the dimensions of the channel, namely channel length 44 and channel width 46. As viewed in a top view, apertures 34, 36 may be in the shape of a square, rectangle, circle, polygon, or any other uniform or non-uniform shape. However, a square aperture is shown in the drawing figures, and used as an example hereinafter. Additionally, the aperture, when viewed from the top, may be entirely or partially enclosed or surrounded by gate 32. For example, the aperture may be located on the

edge of the gate 32 and not entirely enclosed with the gate material resulting in a notch, groove, keyhole, or the like. However, it is currently preferred that the aperture be enclosed within gate 32. The aperture may be formed by conventional mask and etch procedures either before or after the ~~aperture 34~~ gate 32 is formed.

Please amend paragraph [0033] as follows:

[0033] By way of example and not limitation, the relative doping densities as described herein include enhancement implants on the order of E^{12} and LDD implants on the order of E^{12} . Furthermore, DD implants are implanted at, for example, densities on the order of E^{13} while the source and drain regions are implanted at levels on the order of E^{15} . Therefore, it is evident that for ~~short channel~~ short-channel transistors where the LDD and DD structures occupy a significant portion of the channel length, the LDD and DD implants more greatly influence the threshold voltage of the transistor than a threshold voltage adjusting enhancement implant. Embodiments of the present invention enable implanting through the use of apertures distributed about the internal arrangement of the longer gate structures dominating doping densities into the longer channels consistent with the dominant doping densities implanted in shorter channel devices.

Please amend paragraph [0034] as follows:

[0034] To form the source and drain regions, spacers 114, 116 (FIG. 5E) are formed around the gate. With the shallow drain extension junctions protected by the spacers, a second implant with heavier dose is self-aligned to the oxide spacers around the gate to form deep source/drain junctions illustrated as source/drain regions 50, 48. Generally, a rapid thermal annealing occurs (RTA) to enhance the diffusion of the dopants implanted in the deep source/drain junctions. The source/drain implant with heavier doses form low resistance deep drain junctions, which are coupled to the LDD structures. Since the source/drain implant is spaced from the channel by the spacers, the resulting drain junction adjacent to the ~~light~~ lightly

doped drain region can be made deeper without impacting device operation. The increase junction depth lowers the sheet resistance and the contact resistance of the drain.

Please amend paragraph [0039] as follows:

[0039] In an annealing process as depicted in FIG. 5D, the various implantation ions of both the LDD implants 94 and DD implants 104 result in further penetration of the implant ions into substrate 42. As illustrated, the LDD structures (or n- regions) 96-102 as well as the DD implant regions ~~106-112~~ 106-112 migrate under the channel region 52 located under the gate 32. Migration of the higher dopant concentrations of the LDD implants and the DD implants minimizes the impact of the enhancement implant of FIG. 5A and causes the threshold voltage to change according to the additional dopant concentrations.

Please amend paragraph [0040] as follows:

[0040] In FIG. 5E, spacers 114, 116 as well as implant shields 118, 120 protect the underlying structures from the high concentration source/drain implant 122 while the source region 50 and drain region 48 are implanted. As illustrated in FIG. 5F, spacers 114, 116 and implant shields 118, 120 are removed to complete the formation of transistor 30. As illustrated, transistor 30 is comprised of a gate 32, drain and source regions 48, 50 as well as drain and source specific LDD structures 54, 56 and drain and source specific DD structures 62, 64. Transistor 30 further comprises one or more internal LDD structures 58, 60 as well as one or more internal DD structures (or regions) 68, 70. The formation of internal structures, through the use of implants throughout the length of the channel, more consistently aligns the threshold voltage of a ~~long-channel~~ long-channel transistor with the threshold voltage of a ~~short-channel~~ short-channel transistor and thereby reduces the disparate threshold voltages between respective ~~long and short channel~~ long- and short-channel transistors while eliminating independent threshold voltage enhancement implants for ~~long and short channel~~ long- and short-channel transistors.

Please amend paragraph [0041] as follows:

[0041] FIGS. 6 and 7 illustrate grid arrangements of apertures, according to specific embodiments of the present invention. In FIG. 6, the formation of a ~~gate 32~~ gate 134 includes an exemplary pattern of apertures 136 for the gate 134 shown in a “checkerboard” pattern between a source region 138 and a drain region 140. In addition, an exemplary method for calculating the width of aperture 136 with respect to gate 134 height and implantation angle (b) is shown in FIG. 8. One current exemplary embodiment includes a gate length of about 0.1 to 4 microns. FIG. 7 illustrates the formation of apertures in a gate, in accordance with another embodiment of the present invention. A gate 142 includes an exemplary two-dimensional array of apertures 144 located between a source region 146 and a drain region 148. Further geometries and aperture shapes are also contemplated within the scope of the present invention.

Please amend paragraph [0042] as follows:

[0042] FIG. 8 illustrates an exemplary aperture in accordance with an embodiment of the present invention. The dimensions (A) 150 of an aperture 152 may be determined by the gate height, desired ion implantation angle (b) 154, and process or manufacturing capabilities. For example, as shown in FIG. 8, if the gate height is 1200 Å and the desired ion implantation angle (b) 154 is 65°, the dimension (A) 150 would be $(1200\text{Å} / \tan 65^\circ)$ or 560 Å. With current process or manufacturing capabilities, the aperture 152 dimensions are currently preferred to be greater than 0.02 by 0.02 microns. However, the aperture 152 dimension (A) should be small enough to allow the fringe effects from the gate field to electrically invert the charge of the area under the aperture when a voltage is applied to the gate.

Please amend paragraph [0043] as follows:

[0043] The angle (b) 154 shown in FIG. 8 is the angle for driving the dopants into the under layer in the channel region ~~52-(FIG. 5C)-~~ (FIG. 5B). As an example, for a square aperture, this implantation will take place through the device apertures and gate edge and then the device or implantation equipment will be rotated 90° and then the implantation will take place again.

This process will allow for the dopant to be implanted into the channel region 52 of the device on all four sides of a square aperture once a full revolution has been completed. The device or implantation device may turn or rotate more or less times and at a greater or lesser angle to implant the dopant into the channel region 52 depending on the shape of the aperture to get a uniform diffusion under the aperture. Implanting the dopant at the angle (b) 154 will create “fringe” effect regions in the channel region 52 of the device. The angle (a) 156 of the implant at the apertures is currently preferred to be 0 to 25 degrees. The angle is determined by how far the dopant is to be driven under the gate. For example, a small angle (a) 156 will not drive the dopant as far under the gate as a large angle (a) 156 implant. As a result of a smaller angle (a) 156, the fringing of the implant will be reduced in the channel region 52. An exemplary ion implant is phosphorus (Ph) to provide a negative (n-) doping of the channel region 52.

Please amend paragraph [0044] as follows:

[0044] Embodiments of the present invention utilize the implant process for forming one or more of an LDD or a DD region in a short-channel transistor for “enhancing” the concentration of dopants in the channel of a long-channel transistor. Therefore, both the short-channel and ~~long-channel~~ long-channel transistors exhibit similar threshold voltages as adjusted by the LDD and/or DD implanting processes internal to the channel.